FIGS 2-8, further support for the amendments made to Claim 1 is found at Page 6, line 6-Page 9, line 21 of the specification of the instant application.

Insofar as Claim 7 is concerned, applicants have changed the dependency of the claim from Claim 4 to Claim 2.

With regard to Claim 9, applicants have amended that claim to positively recite the structure illustrated in FIG 2. Specifically, applicants have amended Claim 9 to positively recite that a conformal passivation layer is positioned on the exposed sidewalls of the emitter, the patterned insulator layer and the SiGe base region; and that the silicide regions are located on exposed portions of the SiGe layer and the emitter not covered by the conformal passivation layer. In addition to FIG 2, further support for the amendments made to Claim 9 is found at Page 5, line 1-Page 6, line 4 of the specification of the present application.

Since the above amendments to Claims 1, 7 and 9 do not introduce new matter into the specification of the instant application, entry thereof is respectfully requested. Pursuant to 37 C.F.R. §1.121, applicants have attached a marked-up version of the claims showing the changes made by the present amendment. The attachment is captioned as "**MARKED-UP VERSION SHOWING CHANGES MADE**".

In the present Office Action, Claim 1 stands rejected under 35 U.S.C. §102(e) as allegedly anticipated by U.S. Patent No. 6,169,007 to Pinter ("Pinter"). Claims 9, 10, 12, 13, 14, and 15 stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by U.S. Patent No. 5,620,907 to Jalali-Farahani, et al. ("Jalali-Farahani, et al.").

Claims 2 and 5-8 stand rejected under 35 U.S.C. §103 as allegedly unpatentable over the combination of Pinter and U.S. Patent No. 6,319,755 to Halliyal, et al. ("Halliyal, et al."). Claims 3 and 4 stand rejected under 35 U.S.C. §103 as allegedly unpatentable over the

combination of Pinter and U.S. Patent No. 6,326,652 to Rhodes ("Rhodes"). Claim 11 stands rejected under 35 U.S.C. §103 as allegedly unpatentable over the combination of Jalali-Farahani and the publication to A. S. Sedra and K.C. Smith ("Sedra and Smith"), Microelectronic Circuits 1998, Oxford University Press, Inc. Fourth Ed. Claims 16 and 17 stand rejected under 35 U.S.C. §103 as allegedly unpatentable over the combination of Jalali-Farahani and Rhodes.

Applicants respectfully traverse each of the aforementioned §§102 and 103 rejections in view of the amendments made above and the remarks to follow hereineblow.

With regard to the two §102 rejections, it is axiomatic that anticipation under §102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986). Thus, there must be no differences between the subject matter of the claim and the disclosure of the applied prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: The absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants respectfully submit that the disclosure of Pinter does not anticipate Claim 1 of the present application for at least the following reasons: First, Pinter does not disclose a process where a passivation layer is formed on exposed sidewalls of an emitter, insulator layer and portions of a SiGe base region which are all components of a previously formed heterojunction bipolar transistor structure. In contrast, the various insulating layers, including layers 38, 56, 58 and 60, disclosed in Pinter are formed prior to emitter 64 formation. Thus,

none of the insulator layers disclosed in Pinter are formed on exposed sidewalls of a previously formed emitter region.

Additionally, applicants respectfully submit that Pinter does not disclose siliciding any regions of the disclosed heterojunction bipolar transistor structure, let alone siliciding exposed silicon surfaces of at least the emitter and SiGe base region not protected by a passivation layer. Indeed, the term "silicide" does not appear anywhere in the disclosure of Pinter. Applicants respectfully take issue with the Examiner's statement that layers 58, 38 and 36 disclosed in Pinter are silcide layers. Instead, Pinter discloses that layer 58 and 38 are composed of SiO_2, and that layer 38 is a polysilcion region of a PMOS transistor. Applicants find no disclosure in Pinter that regions 58, 38 or 36, or any other for that matter, are composed of a silcide.

With respect to the disclosure of Jalali-Farahani, et al., applicants respectfully submit that the prior art reference does not disclose the SiGe heterojunction bipolar transistor recited in Claims 9, 10, 12, 13, 14 and 15. Specifically, Jalali-Farahani, et al. do not disclose a SiGe heterojunction bipolar transistor which includes a conformal passivation layer positioned on exposed sidewalls of an emitter, a patterned insulator layer and a SiGe base region. Jalali-Farahani, et al. provide a SiGe heterojunction bipolar transistor structure which includes intrinsic 60 and extrinsic base portions 70. The intrinsic base portion comprises epitaxial SiGe alloy and the extrinsic base portion includes a polycrystalline material. Emitter 80 overlies the intrinsic base portion and spacer 100 at least partially overlies the emitter. The prior art structure further includes lower emitter region 110, and silicide contacts 120 and 130 which are present above the emitter region and adjacent to the extrinsic base region. Oxide layer 170 is formed over contact regions 120 and 130.

Applicants respectfully submit that spacer 100, silicide contacts 120 and 130 as well as oxide layer 170 disclosed in Jalali-Farahani, et al. are not a conformal passivation layer that is positioned on exposed sidewalls of an emitter, a patterned insulator layer and a SiGe base region. No such passivation layer, which prevents silicide formation in areas containing the same, is present in the structure disclosed in Jalali-Farahani, et al.

The foregoing remarks clearly indicate that the applied references of Pinter and Jalali-Farahani, et al. do not teach each and every aspect of the claimed invention, as required by King and Kloster Speedsteel; therefore the claims of the present application are not anticipated by either applied reference. Applicants thus respectfully submit that the instant §102(b) and (e) rejections have been obviated; therefore the anticipation rejections can and should be withdrawn.

Insofar as the §103 rejections to method Claims 1-8 are concerned, applicants submit that the combination of Pinter and Halliyal, et al. as well as the combination of Pinter and Rhodes do not teach or suggest applicants' claimed method which includes providing a heterojunction bipolar transistor structure comprising at least an underlying SiGe base region, an insulator layer formed on surface portions of said underlying SiGe base region, and an emitter formed on said insulator layer and in contact with said underlying SiGe base region through an emitter opening formed in said insulator layer, said emitter, said insulator layer and said SiGe base region each having exposed sidewalls; forming a passivation layer on the exposed sidewalls of the emitter, insulator layer and portions of the SiGe base region and siliciding the exposed silicon regions.

The primary reference spurring the §103 rejections, i.e., Pinter, is deficient for the same reasons as mentioned above concerning the §102(e) rejection; therefore those remarks

are incorporated herein by reference. To reiterate: the method disclosed in Pinter does not teach or suggest a process wherein a passivation layer is formed on exposed sidewalls of an emitter, insulator layer and portions of a SiGe base region which are all components of a previously formed heterojunction bipolar transistor structure. In contrast, the various insulating layers, including layers 38, 56, 58 and 60, disclosed in Pinter are formed prior to emitter 64 formation. Thus, none of the insulator layers disclosed in Pinter are formed on sidewalls of a previously formed emitter region.

Additionally, applicants respectfully submit that Pinter does not teach or suggest siliciding any regions of the disclosed heterojunction bipolar transistor structure, let alone siliciding exposed surfaces of at least the emitter and SiGe base region not protected by a passivation layer. Indeed, the term "silicide" does not appear anywhere in the disclosure of Pinter.

The above defects in Pinter are not alleviated by Halliyal or Rhodes since neither of the applied references teaches or suggests applicants' claimed method recited in amended Claim 1. Halliyal, et al. disclose a process for fabricating an ONO floating gate electrode in a two-bit EEPROM device that includes formation of a nitrogenated top oxide layer. Applicants respectfully submits that Halliyal, et al. have nothing to do with forming SiGe heterojunction bipolar transistors, let alone include processing steps wherein a passivation layer is formed on exposed sidewalls of an emitter, insulator layer and portions of a SiGe base region which are all components of a previously formed heterojunction bipolar transistor structure, and thereafter using that passivation layer to prevent formation of silicide regions in areas containing the passivation layer.

Rhodes discloses a CMOS imaging device which includes a buried contact line between the floating diffusion region and the gate of a source follower output transistor. Applicants respectfully submits that Rhodes also has nothing to do with forming SiGe heterojunction bipolar transistors, let alone include processing steps wherein a passivation layer is formed on exposed sidewalls of an emitter, insulator layer and portions of a SiGe base region which are all components of a previously formed heterojunction bipolar transistor structure, and thereafter using that passivation layer to prevent formation of silicide regions in areas containing the passivation layer.

In view of the above amendments and remarks, the instant 103 rejections citing the combinations of Pinter and Halliyal, et al; and Pinter and Rhodes have been obviated. Reconsideration and withdrawal of the instant 103 rejections are thus respectfully requested.

Insofar as the §103 rejections to structure Claims 9-17 are concerned, applicants submit that the combination of Jalali-Farahani, et al. and Sedra and Smith as well as the combination of Jalali-Farahani, et al. and Rhodes do not teach or suggest applicants' claimed structure which includes a conformal passivation layer positioned on exposed sidewalls of an emitter, a patterned insulator layer and a SiGe base region.

The primary reference spurring the §103 rejections, i.e., Jalali-Farahani, et al. is deficient for the same reasons as mentioned above concerning the §102(b) rejection; therefore those remarks are incorporated herein by reference. To reiterate: Jalali-Farahani, et al. do not teach or suggest a SiGe heterojunction bipolar transistor which includes a conformal passivation layer positioned on exposed sidewalls of an emitter, a patterned insulator layer and a SiGe base region. As indicated above, spacer 100, silicide contacts 120 and 130 as well as oxide layer 170 disclosed in Jalali-Farahani, et al. are not a conformal passivation layer that

is positioned on exposed sidewalls of an emitter, a patterned insulator layer and a SiGe base region. No such passivation layer, which prevents silicide formation in areas containing the same, is present in the structure disclosed in Jalali-Farahani, et al.

The above defects in Jalali-Farahani, et al. are not alleviated by Sedra and Smith or Rhodes since neither of the applied references teaches or suggests applicants' claimed structure recited in amended Claim 9. Sedra and Smith disclose CMOS devices such as MOSFETs, resistors, and capacitors; whereas Rhodes discloses a CMOS imaging device which includes a buried contact line between the floating diffusion region and the gate of a source follower output transistor. Applicants respectfully submit that neither Sedra and Smith nor Rhodes has anything to do with SiGe heterojunction bipolar transistors, let alone a SiGe heterojunction dipolar structure which includes a conformal passivation layer positioned on exposed sidewalls of an emitter, a patterned insulator layer and a SiGe base region.

In view of the above amendments and remarks, the instant 103 rejections citing the combinations of Jalali-Farahani, et al. and Sedra and Smith; and Jalali-Farahani, et al. and Rhodes have been obviated. Reconsideration and withdrawal of the instant 103 rejections are thus respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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ATTACHMENT: MARKED-UP VERSION SHOWING CHANGES MADE IN THE CLAIMS:

Please amend Claims 1, 7 and 9 to read as follows:

1. (Amended) A method of improving the SiGe bipolar yield of a SiGe heterojunction bipolar transistor comprising the steps of:

providing a heterojunction bipolar transistor structure comprising at least an underlying SiGe base region, an insulator layer formed on surface portions of said underlying SiGe base region, and an emitter formed on said insulator layer and in contact with said underlying SiGe base region through an emitter opening formed in said insulator layer, said emitter, said insulator layer and said SiGe base region each having exposed sidewalls;

[(a)] forming a passivation layer on [at least] said exposed sidewalls of [an] said emitter, said insulator layer and portions of said SiGe base region[, said emitter is in contact with an underlying SiGe base region through an emitter opening formed in an insulator layer]; and

[(b)] siliciding exposed silicon surfaces of at least said emitter and said SiGe base region not protected by said passivation layer to form silicide regions therein.

7. (Amended) The method of Claim [4] 2 wherein said rapid thermal chemical vapor deposition process is carried out at a temperature of about 700°C or greater.

9. (Amended) A SiGe heterojunction bipolar transistor comprising:

a semiconductor substrate having a collector and subcollector region [formed] located therein, wherein said collector is [formed] located between isolation regions that are also present in the substrate;

a SiGe layer [formed on] atop said substrate, said SiGe layer including polycrystalline Si regions [formed] positioned above said isolation regions and a SiGe base region [formed] located above said collector and subcollector regions;

a patterned insulator layer [formed on] atop said SiGe base region, said patterned insulator having an opening therein;

an emitter [formed] located on said patterned insulator layer and in contact with said SiGe base region through said opening, said emitter, said patterned insulator layer and said SiGe base region each having exposed sidewalls;

a conformal passivation layer [formed on at least said] positioned on said exposed sidewalls of said emitter, said patterned insulator layer and said SiGe base region; and

silicide regions [formed] located on [at least] exposed portions of said SiGe layer and said emitter not covered by said conformal passivation layer.